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Jonathan O. Owens
HAVERSTOCK & OWENS LLP
162 North Wolfe Road
Sunnyvale, CA 94086

EXAMINER	
HOLDER, ANNER N	

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/816,391
Filing Date: March 31, 2004
Appellant(s): DOROJEVETS ET AL.

Jonathan Owens
Reg. No. 37,902
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 03/20/09 appealing from the Office action mailed 12/11/08.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

4,992,933	Taylor	02-1991
5,680,338	Agarwal	10-1997
4,745,547	Buchholz	05-1988

Heaton, Robert " A Bit-Serial VLSI Array Processing Chip for Image Processing" IEEE Journal of Solid-State Circuits, Vol. 25 No. 2, April 1990, pp. 3647-368

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 7, 8, 11, 13-16, 41, 44 and 50-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heaton et al. (Heaton), A Bit-Serial VLSI Array Processing Chip for Image Processing, IEEE Journal of Solid-State Circuits, Vol. 25, No. 2, April 1990.

3. As to claim 1, Heaton teaches a video processing apparatus comprising: a. a memory; [Pg. 365 Col. 2 ¶ 1] and b. one or more video processing modules, each video processing module coupled to the memory and comprising: i. a programmable array of processing elements, each processing element including local registers to provide data used in processing operations and to store results of the processing operations; [Pg. 364 I Introduction; Pg. 364 Col. 2 ¶ 1 – Pg. 366 Col. ¶ 1] ii. a block load and store unit coupled to the programmable array of processing elements to load, store, and send data transferred back and forth between the memory and the array of processing elements; [Pg. 365 Col. 1 ¶ 1 – Pg. 366; Fig. 6; Pg. 366 III Blitzen PE Architecture Col. 1 ¶ 1 - Col. 2 ¶ 1] iii. a global accumulation unit to accumulate the results of the processing operations for each processing element [Fig. 6; Pg. 367 Col. 2 ¶ 1 (sum or tree)] and iv. a local controller to provide instructions and parameters related to the processing operations and data transfer. [Fig. 7; Pg. 364-365 II Blitzen Chip Architecture]

Heaton teaches local accumulation thus it would have been obvious and is fairly suggested by the reference to store results for each processing element in one central location (global accumulation). [Fig. 6; Pg. 367 Col. 2 ¶ 1 (sum or tree); pg 364 I. Introduction]

4. As to claim 2, Heaton teaches the array of processing elements comprises a two-dimensional array. [Fig. 5; Col. 1 ¶ 1 - Col. 2]

5. As to claim 7, Heaton teaches the block load and store unit comprises one or more arrays of exchange registers. [Pg. 365-366 Col. 2 ¶ 1; Fig. 6]

6. As to claim 8, Heaton teaches each array of exchange registers is a two-dimensional array. [Fig. 6 (N Bit Shift Register)]

7. As to claim 11, Heaton teaches a direct, high-bandwidth data path to couple each of the video processing modules to the memory. [Pg. 365 Col. 2 ¶ 1]

8. As to claim 13 Heaton teaches the block load and store unit sends data transferred back and forth between non-adjacent processing elements of the array of processing elements. [Fig. 5; Pg. 365-366 ¶ 1]

9. As to claim 14, Heaton teaches each processing element includes a local accumulation register. [Fig. 6; PG. 366 III Blitzen PE Architecture ¶ 1-3]

10. As to claim 16, Heaton teaches the block load and store unit sends data transferred back and forth between the local registers in the processing elements, the global accumulation unit, and the local controller. [Fig. 6; Pg. 366 Pg. 366 III Blitzen PE Architecture]

11. As to claim 41, Heaton teaches a programmable array of processing elements to process video, each processing element including local registers to store video data blocks received from a main memory, to process the received video data blocks, and to store results of processing the video data blocks, [Fig. 6; Pg. 365 Col. 2 ¶ 1 -Pg. 366 Col. 1 ¶ 2] wherein each processing element is configured to send the results to a

global accumulation unit to accumulate the results of the processing operations for each processing element. [Fig. 6; Pg. 367 Col. 2 ¶ 1 (sum or tree)]

12. As to claim 44, Heaton teaches the array of processing elements comprises a two-dimensional array. [Fig. 5; Col. 1 ¶ 1 - Col. 2]

13. As to claim 50, Heaton each processing element includes a local accumulation register. [Fig. 6; PG. 366 III Blitzen PE Architecture ¶ 1-3]

14. As to claim 51, Heaton each processing element further comprises a plurality of control registers including a PE mask register, a condition register, a block base register, and a vector base register. [Fig. 6; Pg. 366 III Blitzen PE Architecture]

15. Claims 3-4, 9-10, 42-43 and 45-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heaton et al. (Heaton), A Bit-Serial VLSI Array Processing Chip for Image Processing, IEEE Journal of Solid-State Circuits, Vol. 25, No. 2, April 1990 in view of Taylor US 4,992,933.

16. As to claim 3, Heaton teaches the limitations of claim 2.

Heaton does not specifically teach the two-dimensional array comprises a 4X4 ray of processing elements.

Taylor teaches the two-dimensional array comprises a 4X4 ray of processing elements. [Col. 3 Lines 60-67]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Taylor with the device of Heaton, providing array processing elements a greater degree of flexibility. [Taylor Col. 1 Lines 64-66]

17. As to claim 4, Heaton teaches the limitations of claim 2.

Heaton does not specifically the two-dimensional array comprises a single-instruction multiple-data array.

Taylor teaches the two-dimensional array comprises a single-instruction multiple-data array. [Taylor - Abstract; Col. 1 Lines 8-10; Col. 2 Lines 3-12; Col. 31-35]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Taylor with the device of Heaton, providing a SIMD array processing elements an enhanced degree of flexibility. [Taylor Col. 1 Lines 64-66]

18. As to claim 9, Heaton teaches the limitations of claim 1.

Heaton does not specifically teach local controller provides control commands to each processing element, performing control and processing operations on data stored within the local controller, and transfers data between the local controller and other registers within one video module.

Taylor teaches the local controller provides control commands to each processing element, performing control and processing operations on data stored within the local controller, and transfers data between the local controller and other registers within one video module. [Taylor – Fig. 1; Col. 3 Lines 31-39; Col. 4 Lines 7-58; Fig. 2; Fig. 4; Fig. 8]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Taylor with the device of Heaton, allowing for communication and global control of processing elements with in the array.

19. As to claim 10, Heaton (modified by Taylor) teaches a system controller coupled to the memory and to the one or more video processing modules. [Taylor – Fig. 1; Col. 4 Lines 7-58]

20. As to claim 42, Heaton teaches the limitations of claim 41.

Heaton does not specifically teach processing elements coupled to a local controller to provide instructions and parameters related to data transfer and processing of the video data blocks received from the main memory.

Taylor teaches processing elements coupled to a local controller to provide instructions and parameters related to data transfer and processing of the video data blocks received from the main memory. [Abstract; Col. 3 Lines 31-59]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Taylor with the device of Heaton, allowing for communication and global control of processing elements with in the array.

21. As to claim 43, Heaton (modified by Taylor) teaches the limitations of claim the local controller provides control commands to each processing element, performing control and processing operations on data stored within the local controller, and transfers data between the local controller and other registers within one video module. [Taylor – Fig. 1; Col. 3 Lines 31-39; Col. 4 Lines 7-58; Fig. 2; Fig. 4; Fig. 8]

Heaton does not specifically teach processing elements coupled to a local controller to provide instructions and parameters related to data transfer and processing of the video data blocks received from the main memory.

Taylor teaches processing elements coupled to a local controller to provide instructions and parameters related to data transfer and processing of the video data blocks received from the main memory. [Abstract; Col. 3 Lines 31-59]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Taylor with the device of Heaton, providing a SIMD array processing elements an enhanced degree of flexibility. [Taylor Col. 1 Lines 64-66]

22. As to claim 45, Heaton teaches the limitations of claim 44.

Heaton does not specifically teach the two-dimensional array comprises a 4X4 ray of processing elements.

Taylor teaches the two-dimensional array comprises a 4X4 ray of processing elements. [Col. 3 Lines 60-67]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Taylor with the device of Heaton, providing array processing elements a greater degree of flexibility. [Taylor Col. 1 Lines 64-66]

23. As to claim 46, Heaton teaches the limitations of claim 2.

Heaton does not specifically the two-dimensional array comprises a single-instruction multiple-data array.

Taylor teaches the two-dimensional array comprises a single-instruction multiple-data array. [Taylor - Abstract; Col. 1 Lines 8-10; Col. 2 Lines 3-12; Col. 31-35]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Taylor with the device of Heaton, providing a

SIMD array processing elements an enhanced degree of flexibility. [Taylor Col. 1 Lines 64-66]

24. Claims 12 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heaton et al. (Heaton), A Bit-Serial VLSI Array Processing Chip for Image Processing, IEEE Journal of Solid-State Circuits, Vol. 25, No. 2, April 1990 in view of Buchholz et al. (Buchholz) US 4,745,547.

25. As to claim 12, Heaton teaches the limitations of claim 1.

Heaton does not specifically teach each processing element further comprises a plurality of scalar registers.

Buchholz teaches a plurality of scalar registers. [Col. 6 Lines 5-8]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Buchholz with the device of Heaton allowing improvements to image processing.

26. As to claim 49, see the rejection of 12.

27. Claims 5-6, 15 and 47-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heaton et al. (Heaton), A Bit-Serial VLSI Array Processing Chip for Image Processing, IEEE Journal of Solid-State Circuits, Vol. 25, No. 2, April 1990 in view of Agarwal et al. (Agarwal) US 5,680,338.

28. As to claim 5, Heaton teaches each processing element includes a plurality of block registers. [Heaton – Fig. 6; Pg. 366 III Blitzen PE Architecture Col. 1 ¶ 1- Col. 2 ¶ 2 (memory registers)]

Heaton does not specifically teach vector registers.

Agarwal teaches vector registers. [Figs. 2-4; Col. 6 Lines 16-33, 57-65]

It would have been obvious to one of ordinary skill in the art to incorporate the teachings of Agarwal in the device of Heaton, allowing for improvements in image processing and image quality.

29. As to claim 6, Heaton (modified by Agarwal) teaches each block register is configured to hold 8 8-bit data elements as a two-dimensional 2X4 block of pixels or 4 16-bit data elements as a one-dimensional vector. [Agarwal - Figs. 2-4; Col. 6 Lines 16-33, 57-65]

30. As to claim 15, Heaton (modified by Agarwal) teaches each processing element further comprises a plurality of control registers including a PE mask register, a condition register, a block base register, and a vector base register. [Heaton - Fig. 6; Pg. 366 III Blitzen PE Architecture; Agarwal - Figs. 2-4; Col. 6 Lines 16-33, 57-65]

31. As to claim 47, Heaton (modified by Agarwal) teaches each processing element includes a plurality of vector registers and a plurality of block registers. . [Heaton – Fig. 6; Pg. 366 III Blitzen PE Architecture Col. 1 ¶ 1- Col. 2 ¶ 2 (memory registers)]

Heaton does not specifically teach vector registers.

Agarwal teaches vector registers. [Figs. 2-4; Col. 6 Lines 16-33, 57-65]

It would have been obvious to one of ordinary skill in the art to incorporate the teachings of Agarwal in the device of Heaton, allowing for improvements in image processing and image quality.

32. As to claim 48, Heaton (modified by Agarwal) teaches each vector register and each block register is configured to hold 8 8-bit data elements as a two-dimensional

2.times.4 block of pixels or 4 16-bit data elements as a one-dimensional vector. [Agarwal - Figs. 2-4; Col. 6 Lines 16-33, 57-65]

33. Claims 17-26, 28, 29-38, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heaton et al. (Heaton), A Bit-Serial VLSI Array Processing Chip for Image Processing, IEEE Journal of Solid-State Circuits, Vol. 25, No. 2, April 1990 in view of Taylor US 4,992,933 further in view of Agarwal et al. (Agarwal) US 5,680,338.

34. As to claim 17, Heaton teaches a method of processing video comprising: a. configuring a video stream into data blocks; [Fig. 3; Pg. 365-366 Col. 1 ¶ 1] b. loading data blocks from memory to a first array of exchange registers; [Fig. 6 (shift registers)] c. loading data blocks from the first array of exchange registers to a programmable array of processing elements, wherein each processing element within the array of processing elements includes an array of block registers, an array of vector registers, and a local accumulator, the data blocks are loaded from the first array of exchange registers to the array of block registers; [Fig. 6; Pg. 366 III Blitzen PE Architecture Col. 1 ¶ 1 – Col. 2 ¶ 1] e. processing the data blocks loaded in the array of vector registers and storing results in the corresponding local accumulator for each processing element; [Fig. 6; Pg. 365-366] f. accumulating the results stored in the local accumulators in a global accumulator, thereby forming accumulated results. [Fig. 6; Pg. 367 Col. 2 ¶ 1 (sum or tree)]

Heaton does not specifically teach moving the results into a local controller.

Taylor teaches moving the results into a local controller. [Abstract; Fig. 1; Col. 5 Lines 22-28]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Taylor with the device of Heaton, providing array processing elements an enhanced degree of flexibility. [Taylor Col. 1 Lines 64-66]

Heaton (Modified Taylor) does not specifically teach loading the data blocks from the array of block registers to the array of vector registers.

Agarwal teaches loading the data blocks from the array of block registers to the array of vector registers. [Col. 4 Lines 37-49; Col. 5 Lines 45-59; Figs. 2-4; Col. 6 Lines 16-33, 57-65]

It would have been obvious to one of ordinary skill in the art to incorporate the teachings of Agarwal in the device of Heaton modified by Taylor, allowing for improvements in image processing and image quality.

35. As to claim 18, Heaton (modified by Taylor and Agarwal) teaches storing results from processing the data blocks in the array of vector registers, and loading the results stored in the array of vector registers in the array of block registers. [Heaton – Fig. 6; Pg. 366 III Blitzen PE Architecture Col. 1 ¶ 1- Col. 2 ¶ 2 (memory registers); Agarwal - Col. 4 Lines 37-49; Col. 5 Lines 45-59; Figs. 2-4; Col. 6 Lines 16-33, 57-65]

36. As to claim 19, Heaton (modified by Taylor and Agarwal) teaches loading the results in the array of block registers into a second array of exchange registers, and loading the results from the array of block registers into memory. [Taylor – Fig.1; Fig. 2; Col. 5 Lines 18-28; Heaton – Fig. 6; Pg. 366 III Blitzen PE Architecture Col. 1 ¶ 1- Col. 2 ¶ 2]

37. As to claim 20, Heaton (modified by Taylor and Agarwal) teaches each of the first and second array of exchange registers is a two-dimensional array. [Heaton – Fig. 6; Pg. 366 III Blitzen PE Architecture Col. 1 ¶ 1- Col. 2 ¶ 2; Fig. 5; Pg. 365-366 Col. 2 ¶ 1]

38. As to claim 21, Heaton (modified by Taylor and Agarwal) teaches loading the results in the array of block registers into a second array of exchange registers, and loading the results in the second array of exchange registers into another array of block registers included within non-adjacent processing elements to the processing elements including the array of block registers. [Heaton – Fig. 6; Pg. 366 III Blitzen PE Architecture Col. 1 ¶ 1- Col. 2 ¶ 2; Fig. 5; Pg. 365-366 Col. 2 ¶ 1]

39. As to claim 22, Heaton (modified by Taylor and Agarwal) teaches loading the results in the array of block registers into another array of block registers included within a processing element adjacent to the processing element including the array of block registers. Heaton – Fig. 6; Pg. 366 III Blitzen PE Architecture Col. 1 ¶ 1- Col. 2 ¶ 2; Fig. 5; Pg. 365-366 Col. 2 ¶ 1]

40. As to claim 23, Heaton (modified by Taylor and Agarwal) teaches the array of processing elements comprises a two-dimensional array. [Heaton - Fig. 5; Col. 1 ¶ 1 - Col. 2]

41. As to claim 24, Heaton (modified by Taylor and Agarwal) teaches the two-dimensional array comprises a 4X4 array of processing elements. [Taylor - Col. 3 Lines 60-67]

42. As to claim 25, Heaton (modified by Taylor and Agarwal) teaches the two-dimensional array comprises a single-instruction multiple-data array. [Agarwal - Figs. 2-4; Col. 6 Lines 16-33, 57-65]

43. As to claim 26, Heaton (modified by Taylor and Agarwal) teaches each vector register and each block register is configured to hold 8 8-bit data elements as a two-dimensional 2X4 block of pixels or 4 16-bit data elements as a one-dimensional vector. [Agarwal - Figs. 2-4; Col. 6 Lines 16-33, 57-65]

44. As to claim 28, Heaton (modified by Taylor and Agarwal) teaches the local controller utilizes the accumulated results to make control decisions related to video processing. [Taylor – Abstract; Col. 3 Lines 31-59; Heaton - Pg. 367 Col. 2 ¶ 1]

45. As to claim 29, see rejection of claim 17 above.

46. As to claim 30, see rejection of claim 18 above.

47. As to claim 31, see rejection of claim 19 above.

48. As to claim 32, see the rejection of claim 20 above.

49. As to claim 33, see rejection of claim 21 above.

50. As to claim 34, see rejection of claim 22 above.

51. As to claim 35, see rejection of claim 23 above.

52. As to claim 36, see rejection of claim 24 above.

53. As to claim 37, see rejection of claim 25 above.

54. As to claim 38, see rejection of claim 26 above.

55. As to claim 40, see rejection of claim 28 above.

56. Claim 27 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heaton et al. (Heaton), A Bit-Serial VLSI Array Processing Chip for Image Processing, IEEE Journal of Solid-State Circuits, Vol. 25, No. 2, April 1990 in view of Taylor US 4,992,933 in view of Agarwal et al. (Agarwal) US 5,680,338 further in view Buchholz et al. (Buchholz) US 4,745,547.

57. As to claim 27, Heaton teaches that processing the data blocks includes processing data blocks loaded from the array of block registers and data loaded from the array of scalar registers. [Fig. 5; Pg. 365 Col. 1 ¶ 1 – Pg. 366; Fig. 6; Pg. 366 III Blitzen PE Architecture Col. 1 ¶ 1 - Col. 2 ¶ 1; teaches the loading and transfer from elements including registers)]

Heaton does not specifically teach each processing element further comprises a plurality of scalar registers.

Buchholz teaches a plurality of scalar registers. [Col. 6 Lines 5-8]

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Buchholz with the device of Heaton allowing improvements to image processing.

58. As to claim 39, see rejection of claim 27 above.

(10) Response to Argument

Appellant's arguments filed 03/20/09 with respect to claims 1-51 have been fully considered but they are not persuasive.

The Appellants eighteen arguments contending the Examiner's rejection of claims 1-2, 7, 8, 11, 13-16, 41, 44 and 50-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heaton et al. (Heaton), A Bit-Serial VLSI Array Processing Chip for Image Processing, IEEE Journal of Solid-State Circuits, Vol. 25, No. 2, April 1990; claims 3-4, 9-10, 42-43 and 45-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heaton et al. (Heaton), A Bit-Serial VLSI Array Processing Chip for Image Processing, IEEE Journal of Solid-State Circuits, Vol. 25, No. 2, April 1990 in view of Taylor US 4,992,933; claims 12 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heaton et al. (Heaton), A Bit-Serial VLSI Array Processing Chip for Image Processing, IEEE Journal of Solid-State Circuits, Vol. 25, No. 2, April 1990 in view of Buchholz et al. (Buchholz) US 4,745,547; claims 5-6, 15 and 47-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heaton et al. (Heaton), A Bit-Serial VLSI Array Processing Chip for Image Processing, IEEE Journal of Solid-State Circuits, Vol. 25, No. 2, April 1990 in view of Agarwal et al. (Agarwal) US 5,680,338; claims 17-26, 28, 29-38, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heaton et al. (Heaton), A Bit-Serial VLSI Array Processing Chip for Image Processing, IEEE Journal of Solid-State Circuits, Vol. 25, No. 2, April 1990 in view of Taylor US 4,992,933 further in view of Agarwal et al. (Agarwal) US

5,680,338; claim 27 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heaton et al. (Heaton), A Bit-Serial VLSI Array Processing Chip for Image Processing, IEEE Journal of Solid-State Circuits, Vol. 25, No. 2, April 1990 in view of Taylor US 4,992,933 in view of Agarwal et al. (Agarwal) US 5,680,338 further in view Buchholz et al. (Buchholz) US 4,745,547. However, after a careful consideration of numerous arguments, the Examiner must respectfully disagree for the reasons that follow, and submit to the Board that the rejections are proper and should be maintained.

The Appellant argues that Heaton fails to disclose "a global accumulation unit to accumulate the results of the processing operations for each processing elements." [Brief of 03/20/09: page 6 lines 28-29; page 7 lines 1-2; page 9 lines 28-30; page 10 lines 11-13; page 15 line 12] The Examiner respectfully disagrees. Accordingly, the Examiner maintains that Heaton meets the limitations of the claims. Heaton discloses in fig 6 a global address which is provided to the local processing element. The presence of a global address is an indication of then processing elements are accumulating on a global scale. Further, Heaton specifies that each processing element performs the global operations. [Heaton: page 364 I. Introduction line 16; page 367 second column lines 3-4] Appellant argues that additional adders and a shift register would be required to perform global accumulation to accumulate the results of the processing operations of each processing element. [Brief: page 15 lines 3-8] The Examiner would like to point out that Heaton discloses a global accumulation for each processing element [Heaton: page 364 I. Introduction line 16] meeting the limitations of Appellant's claim 1 step 3.

[Brief: page 20 lines 15-16] Being that step 3 of Appellant claim limitation as written corresponds to a global operation within each processing element.

As to claims 1, 2, 7, 8, 11, 13-16 the Appellant argues that Heaton fails to disclose "a global accumulation unit to accumulate the results of the processing operations for each processing elements." [Brief of 03/20/09: page 6 lines 28-29; page 7 lines 1-2; page 9 lines 28-30; page 10 lines 11-13; page 15 line 12] The Examiner respectfully disagrees. Accordingly, the Examiner maintains that Heaton meets the limitations of the claims. Heaton discloses in fig 6 a global address which is provided to the local processing element. The presence of a global address is an indication of then processing elements are accumulating on a global scale. Further, Heaton specifies that each processing element performs the global operations. [Heaton: page 364 I. Introduction line 16; page 367 second column lines 3-4] Appellant argues that additional adders and a shift register would be required to perform global accumulation to accumulate the results of the processing operations of each processing element. [Brief: page 15 lines 3-8] The Examiner would like to point out that Heaton discloses a global accumulation for each processing element [Heaton: page 364 I. Introduction line 16] meeting the limitations of Appellant's claim 1 step 3. [Brief: page 20 lines 15-16] Being that step 3 of Appellant claim limitation as written corresponds to a global operation within each processing element. Claims 2, 7, 8, 11, 13-16 are not considered to stand and fall independently Appellant has repeated the argument provided for claim 1. A separate argument must be provided and argued for each claim.

As to claims 41, 44, 50 and 51 the Appellant argues that Heaton fails to disclose "a global accumulation unit to accumulate the results of the processing operations for each processing elements." [Brief of 03/20/09: page 6 lines 28-29; page 7 lines 1-2; page 9 lines 28-30; page 10 lines 11-13; page 15 line 12] The Examiner respectfully disagrees. Accordingly, the Examiner maintains that Heaton meets the limitations of the claims. Heaton discloses in fig 6 a global address which is provided to the local processing element. The presence of a global address is an indication of then processing elements are accumulating on a global scale. Further, Heaton specifies that each processing element performs the global operations. [Heaton: page 364 I. Introduction line 16; page 367 second column lines 3-4] The Examiner would like to point out that Heaton discloses a global accumulation for each processing element [Heaton: page 364 I. Introduction line 16] meeting the limitation of Appellant's claim 41. [Brief: page 26 lines 11-12] Claims 44, 50 and 51 are not considered to stand and fall independently Appellant has repeated the argument provided for claim 41. A separate argument must be provided and argued for each claim.

As to claims 3, 4, 9 and 10 the appellant argues all are dependant on claim 1. Regarding claim 1 Appellant argues that Heaton fails to disclose "a global accumulation unit to accumulate the results of the processing operations for each processing elements." [Brief of 03/20/09: page 6 lines 28-29; page 7 lines 1-2; page 9 lines 28-30; page 10 lines 11-13; page 15 line 12] The Examiner respectfully disagrees. Accordingly, the Examiner maintains that Heaton meets the limitations of the claims. Heaton discloses in fig 6 a global address which is provided to the local processing element.

The presence of a global address is an indication of then processing elements are accumulating on a global scale. Further, Heaton specifies that each processing element performs the global operations. [Heaton: page 364 I. Introduction line 16; page 367 second column lines 3-4] Appellant argues that additional adders and a shift register would be required to perform global accumulation to accumulate the results of the processing operations of each processing element. [Brief: page 15 lines 3-8] The Examiner would like to point out that Heaton discloses a global accumulation for each processing element [Heaton: page 364 I. Introduction line 16] meeting the limitations of Appellant's claim 1 step 3. [Brief: page 20 lines 15-16] Being that step 3 of Appellant claim limitation as written corresponds to a global operation within each processing element. Claims 3, 4, 9 and 10 are not considered to stand and fall independently Appellant dependants upon the arguments provided for claim 1. A separate argument must be provided and argued for each claim.

As to claims 43, 43, 45, and 46 the Appellant argues all are dependant on claim 1. Regarding claim 41 the Appellant argues that Heaton fails to disclose "a global accumulation unit to accumulate the results of the processing operations for each processing elements." [Brief of 03/20/09: page 6 lines 28-29; page 7 lines 1-2; page 9 lines 28-30; page 10 lines 11-13; page 15 line 12] The Examiner respectfully disagrees. Accordingly, the Examiner maintains that Heaton meets the limitations of the claims. Heaton discloses in fig 6 a global address which is provided to the local processing element. The presence of a global address is an indication of then processing elements are accumulating on a global scale. Further, Heaton specifies that each processing

element performs the global operations. [Heaton: page 364 I. Introduction line 16; page 367 second column lines 3-4] The Examiner would like to point out that Heaton discloses a global accumulation for each processing element [Heaton: page 364 I. Introduction line 16] meeting the limitation of Appellant's claim 41. [Brief: page 26 lines 11-12] Claims 43, 43, 45, and 46 are not considered to stand and fall independently Appellant dependants upon the arguments provided for claim 41. A separate argument must be provided and argued for each claim.

As to claim 12 the Appellant argues dependency on claim 1. Regarding claim 1 Appellant argues that Heaton fails to disclose "a global accumulation unit to accumulate the results of the processing operations for each processing elements." [Brief of 03/20/09: page 6 lines 28-29; page 7 lines 1-2; page 9 lines 28-30; page 10 lines 11-13; page 15 line 12] The Examiner respectfully disagrees. Accordingly, the Examiner maintains that Heaton meets the limitations of the claims. Heaton discloses in fig 6 a global address which is provided to the local processing element. The presence of a global address is an indication of then processing elements are accumulating on a global scale. Further, Heaton specifies that each processing element performs the global operations. [Heaton: page 364 I. Introduction line 16; page 367 second column lines 3-4] Appellant argues that additional adders and a shift register would be required to perform global accumulation to accumulate the results of the processing operations of each processing element. [Brief: page 15 lines 3-8] The Examiner would like to point out that Heaton discloses a global accumulation for each processing element [Heaton: page 364 I. Introduction line 16] meeting the limitations of Appellant's claim 1 step 3.

[Brief: page 20 lines 15-16] Being that step 3 of Appellant claim limitation as written corresponds to a global operation within each processing element. Claim 12 is not considered to stand and fall independently Appellant dependants upon the arguments provided for claim 1. A separate argument must be provided and argued for each claim.

As to claim 49 the Appellant argues dependency on claim 41. Regarding claim 41 the Appellant argues that Heaton fails to disclose "a global accumulation unit to accumulate the results of the processing operations for each processing elements." [Brief of 03/20/09: page 6 lines 28-29; page 7 lines 1-2; page 9 lines 28-30; page 10 lines 11-13; page 15 line 12] The Examiner respectfully disagrees. Accordingly, the Examiner maintains that Heaton meets the limitations of the claims. Heaton discloses in fig 6 a global address which is provided to the local processing element. The presence of a global address is an indication of then processing elements are accumulating on a global scale. Further, Heaton specifies that each processing element performs the global operations. [Heaton: page 364 I. Introduction line 16; page 367 second column lines 3-4] The Examiner would like to point out that Heaton discloses a global accumulation for each processing element [Heaton: page 364 I. Introduction line 16] meeting the limitation of Appellant's claim 41. [Brief: page 26 lines 11-12] Claim 49 is not considered to stand and fall independently Appellant dependants upon the arguments provided for claim 41. A separate argument must be provided and argued for each claim.

As to claims 5, 6, 15 he Appellant argues dependency on claim 1. Regarding claim 1 Appellant argues that Heaton fails to disclose "a global accumulation unit to accumulate the results of the processing operations for each processing elements." [Brief of 03/20/09: page 6 lines 28-29; page 7 lines 1-2; page 9 lines 28-30; page 10 lines 11-13; page 15 line 12] The Examiner respectfully disagrees. Accordingly, the Examiner maintains that Heaton meets the limitations of the claims. Heaton discloses in fig 6 a global address which is provided to the local processing element. The presence of a global address is an indication of then processing elements are accumulating on a global scale. Further, Heaton specifies that each processing element performs the global operations. [Heaton: page 364 I. Introduction line 16; page 367 second column lines 3-4] Appellant argues that additional adders and a shift register would be required to perform global accumulation to accumulate the results of the processing operations of each processing element. [Brief: page 15 lines 3-8] The Examiner would like to point out that Heaton discloses a global accumulation for each processing element [Heaton: page 364 I. Introduction line 16] meeting the limitations of Appellant's claim 1 step 3. [Brief: page 20 lines 15-16] Being that step 3 of Appellant claim limitation as written corresponds to a global operation within each processing element. Claims 5, 6, 15 are not considered to stand and fall independently Appellant dependants upon the arguments provided for claim 1. A separate argument must be provided and argued for each claim.

As to claim 47 and 49 the Appellant argues dependency on claim 41. Regarding claim 41 the Appellant argues that Heaton fails to disclose "a global accumulation unit to

accumulate the results of the processing operations for each processing elements." [Brief of 03/20/09: page 6 lines 28-29; page 7 lines 1-2; page 9 lines 28-30; page 10 lines 11-13; page 15 line 12] The Examiner respectfully disagrees. Accordingly, the Examiner maintains that Heaton meets the limitations of the claims. Heaton discloses in fig 6 a global address which is provided to the local processing element. The presence of a global address is an indication of then processing elements are accumulating on a global scale. Further, Heaton specifies that each processing element performs the global operations. [Heaton: page 364 I. Introduction line 16; page 367 second column lines 3-4] The Examiner would like to point out that Heaton discloses a global accumulation for each processing element [Heaton: page 364 I. Introduction line 16] meeting the limitation of Appellant's claim 41. [Brief: page 26 lines 11-12] Claims 47 and 48 are not considered to stand and fall independently Appellant dependants upon the arguments provided for claim 41. A separate argument must be provided and argued for each claim.

In addition Appellant argues Heaton taken in combination with Taylor and Agarwal fails to teach "a global accumulation unit to accumulate the results of the processing operations for each processing element." [Brief: page 12 lines 25-29; page 13 lines 1-4] The Examiner respectfully disagrees. Accordingly, the Examiner maintains that Heaton meets the limitations of the claims. Heaton discloses in fig 6 a global address which is provided to the local processing element. The presence of a global address is an indication of then processing elements are accumulating on a global scale. Further, Heaton specifies that each processing element performs the global operations. [Heaton:

page 364 I. Introduction line 16; page 367 second column lines 3-4] Appellant argues that additional adders and a shift register would be required to perform global accumulation to accumulate the results of the processing operations of each processing element. [Brief: page 15 lines 3-8] The Examiner would like to point out that Heaton discloses a global accumulation for each processing element [Heaton: page 364 I. Introduction line 16] meeting the limitations of Appellant's claim 17 step f. [Brief: page 22 lines 21-22] Taylor is incorporated for the teaching and disclosure of moving the results into a local controller. [Abstract; Fig. 1; Col. 5 Lines 22-28] The combination of the teachings of Taylor with the device of Heaton, provides array processing elements an enhanced degree of flexibility. [Taylor Col. 1 Lines 64-66] Additionally Agarwal is combined for teaching and disclosure of loading the data blocks from the array of block registers to the array of vector registers. [Col. 4 Lines 37-49; Col. 5 Lines 45-59; Figs. 2-4; Col. 6 Lines 16-33, 57-65] the incorporating of the teachings of Agarwal in the device of Heaton modified by Taylor, allows for improvements in image processing and image quality.

Appellant argues that Taylor does not teach a global accumulation unit to accumulate the results of the processing operations for each processing element. The Examiner would like point out that Heaton discloses in fig 6 a global address which is provided to the local processing element. The presence of a global address is an indication of then processing elements are accumulating on a global scale. Further, Heaton specifies that each processing element performs the global operations. [Heaton: page 364 I. Introduction line 16; page 367 second column lines 3-4] Appellant argues that additional

adders and a shift register would be required to perform global accumulation to accumulate the results of the processing operations of each processing element. [Brief: page 15 lines 3-8] The Examiner would like to point out that Heaton discloses a global accumulation for each processing element [Heaton: page 364 I. Introduction line 16] meeting the limitations of Appellant's claim 17 step f. [Brief: page 22 lines 21-22] Taylor is provided to cure deficiencies in Heaton regarding two dimensional arrays, local controllers, and moving the results into a local controller.

Appellant argues that Agarwal does not teach a global accumulation unit to accumulate the results of the processing operations for each processing element. The Examiner would like point out that Heaton discloses in fig 6 a global address which is provided to the local processing element. The presence of a global address is an indication of then processing elements are accumulating on a global scale. Further, Heaton specifies that each processing element performs the global operations. [Heaton: page 364 I. Introduction line 16; page 367 second column lines 3-4] Appellant argues that additional adders and a shift register would be required to perform global accumulation to accumulate the results of the processing operations of each processing element. [Brief: page 15 lines 3-8] The Examiner would like to point out that Heaton discloses a global accumulation for each processing element [Heaton: page 364 I. Introduction line 16] meeting the limitations of Appellant's claim 17 step f. [Brief: page 22 lines 21-22] Agarwal is provided to cure deficiencies in Heaton regarding loading the data blocks from the array of block registers to the array of vector registers.

Further, Appellant argues Heaton taken in combination with Taylor and Agarwal fails to teach "a global accumulation unit to accumulate the results of the processing operations for each processing element." [Brief: page 12 lines 25-29; page 13 lines 1-4; page 16 lines 4-6] The Examiner respectfully disagrees. Accordingly, the Examiner maintains that Heaton meets the limitations of the claims. Heaton discloses in fig 6 a global address which is provided to the local processing element. The presence of a global address is an indication of then processing elements are accumulating on a global scale. Further, Heaton specifies that each processing element performs the global operations. [Heaton: page 364 I. Introduction line 16; page 367 second column lines 3-4] Appellant argues that additional adders and a shift register would be required to perform global accumulation to accumulate the results of the processing operations of each processing element. [Brief: page 15 lines 3-8] The Examiner would like to point out that Heaton discloses a global accumulation for each processing element [Heaton: page 364 I. Introduction line 16] meeting the limitations of Appellant's claim 17 step f. [Brief: page 22 lines 21-22] Taylor is incorporated for the teaching and disclosure of moving the results into a local controller. [Abstract; Fig. 1; Col. 5 Lines 22-28] The combination of the teachings of Taylor with the device of Heaton, provides array processing elements an enhanced degree of flexibility. [Taylor Col. 1 Lines 64-66] Additionally Agarwal is combined for teaching and disclosure of loading the data blocks from the array of block registers to the array of vector registers. [Col. 4 Lines 37-49; Col. 5 Lines 45-59; Figs. 2-4; Col. 6 Lines 16-33, 57-65] the incorporating of the teachings of

Agarwal in the device of Heaton modified by Taylor, allows for improvements in image processing and image quality.

As to claim 17 Appellant argues Heaton taken in combination with Taylor and Agarwal fails to teach "accumulating the results stored in the local accumulators in a global accumulator, thereby forming accumulated results." [Brief: page 17 lines 2-4] The Examiner respectfully disagrees. Accordingly, the Examiner maintains that Heaton meets the limitations of the claims. Heaton discloses in fig 6 a global address which is provided to the local processing element. The presence of a global address is an indication of then processing elements are accumulating on a global scale. Further, Heaton specifies that each processing element performs the global operations. [Heaton: page 364 I. Introduction line 16; page 367 second column lines 3-4] Appellant argues that additional adders and a shift register would be required to perform global accumulation to accumulate the results of the processing operations of each processing element. [Brief: page 15 lines 3-8] The Examiner would like to point out that Heaton discloses a global accumulation for each processing element [Heaton: page 364 I. Introduction line 16] meeting the limitations of Appellant's claim 17 step f. [Brief: page 22 lines 21-22] Taylor is incorporated for the teaching and disclosure of moving the results into a local controller. [Abstract; Fig. 1; Col. 5 Lines 22-28] The combination of the teachings of Taylor with the device of Heaton, provides array processing elements an enhanced degree of flexibility. [Taylor Col. 1 Lines 64-66] Additionally Agarwal is combined for teaching and disclosure of loading the data blocks from the array of block registers to the array of vector registers. [Col. 4 Lines 37-49; Col. 5 Lines 45-59; Figs. 2-

4; Col. 6 Lines 16-33, 57-65] the incorporating of the teachings of Agarwal in the device of Heaton modified by Taylor, allows for improvements in image processing and image quality. Claims 18-26 and 28 are not considered to stand and fall independently Appellant has repeated the argument provided for claim 17. A separate argument must be provided and argued for each claim.

As to claims 29-38 and 40 Appellant argues Heaton taken in combination with Taylor and Agarwal fails to teach "accumulating the results stored in the local accumulators in a global accumulator, thereby forming accumulated results." [Brief: page 17 lines 2-4] The Examiner respectfully disagrees. Accordingly, the Examiner maintains that Heaton meets the limitations of the claims. Heaton discloses in fig 6 a global address which is provided to the local processing element. The presence of a global address is an indication of then processing elements are accumulating on a global scale. Further, Heaton specifies that each processing element performs the global operations. [Heaton: page 364 I. Introduction line 16; page 367 second column lines 3-4] Appellant argues that additional adders and a shift register would be required to perform global accumulation to accumulate the results of the processing operations of each processing element. [Brief: page 15 lines 3-8] The Examiner would like to point out that Heaton discloses a global accumulation for each processing element [Heaton: page 364 I. Introduction line 16] meeting the limitations of Appellant's claim 29 step f. [Brief: page 24 lines 21-23] Taylor is incorporated for the teaching and disclosure of moving the results into a local controller. [Abstract; Fig. 1; Col. 5 Lines 22-28] The combination of the teachings of Taylor with the device of Heaton, provides array processing elements an

enhanced degree of flexibility. [Taylor Col. 1 Lines 64-66] Additionally Agarwal is combined for teaching and disclosure of loading the data blocks from the array of block registers to the array of vector registers. [Col. 4 Lines 37-49; Col. 5 Lines 45-59; Figs. 2-4; Col. 6 Lines 16-33, 57-65] the incorporating of the teachings of Agarwal in the device of Heaton modified by Taylor, allows for improvements in image processing and image quality. Claims 30-38 and 40 are not considered to stand and fall independently Appellant has repeated the argument provided for claim 29. A separate argument must be provided and argued for each claim.

As to claim 39 the Appellant argues dependency on claim 29. Regarding claim 29 the Appellant argues Heaton taken in combination with Taylor and Agarwal fails to teach "accumulating the results stored in the local accumulators in a global accumulator, thereby forming accumulated results." [Brief: page 17 lines 2-4] The Examiner respectfully disagrees. Accordingly, the Examiner maintains that Heaton meets the limitations of the claims. Heaton discloses in fig 6 a global address which is provided to the local processing element. The presence of a global address is an indication of then processing elements are accumulating on a global scale. Further, Heaton specifies that each processing element performs the global operations. [Heaton: page 364 I. Introduction line 16; page 367 second column lines 3-4] Appellant argues that additional adders and a shift register would be required to perform global accumulation to accumulate the results of the processing operations of each processing element. [Brief: page 15 lines 3-8] The Examiner would like to point out that Heaton discloses a global accumulation for each processing element [Heaton: page 364 I. Introduction line 16]

meeting the limitations of Appellant's claim 17 step f. [Brief: page 22 lines 21-22] Taylor is incorporated for the teaching and disclosure of moving the results into a local controller. [Abstract; Fig. 1; Col. 5 Lines 22-28] The combination of the teachings of Taylor with the device of Heaton, provides array processing elements an enhanced degree of flexibility. [Taylor Col. 1 Lines 64-66] Additionally Agarwal is combined for teaching and disclosure of loading the data blocks from the array of block registers to the array of vector registers. [Col. 4 Lines 37-49; Col. 5 Lines 45-59; Figs. 2-4; Col. 6 Lines 16-33, 57-65] the incorporating of the teachings of Agarwal in the device of Heaton modified by Taylor, allows for improvements in image processing and image quality. Claim 27 is not considered to stand and fall independently Appellant has repeated the argument provided for claim 17. A separate argument must be provided and argued for each claim.

As to claims 29-38 and 40 Appellant argues Heaton taken in combination with Taylor and Agarwal fails to teach "accumulating the results stored in the local accumulators in a global accumulator, thereby forming accumulated results." [Brief: page 17 lines 2-4] The Examiner respectfully disagrees. Accordingly, the Examiner maintains that Heaton meets the limitations of the claims. Heaton discloses in fig 6 a global address which is provided to the local processing element. The presence of a global address is an indication of then processing elements are accumulating on a global scale. Further, Heaton specifies that each processing element performs the global operations. [Heaton: page 364 I. Introduction line 16; page 367 second column lines 3-4] Appellant argues that additional adders and a shift register would be required to perform global

accumulation to accumulate the results of the processing operations of each processing element. [Brief: page 15 lines 3-8] The Examiner would like to point out that Heaton discloses a global accumulation for each processing element [Heaton: page 364 I. Introduction line 16] meeting the limitations of Appellant's claim 29 step f. [Brief: page 24 lines 21-23] Taylor is incorporated for the teaching and disclosure of moving the results into a local controller. [Abstract; Fig. 1; Col. 5 Lines 22-28] The combination of the teachings of Taylor with the device of Heaton, provides array processing elements an enhanced degree of flexibility. [Taylor Col. 1 Lines 64-66] Additionally Agarwal is combined for teaching and disclosure of loading the data blocks from the array of block registers to the array of vector registers. [Col. 4 Lines 37-49; Col. 5 Lines 45-59; Figs. 2-4; Col. 6 Lines 16-33, 57-65] the incorporating of the teachings of Agarwal in the device of Heaton modified by Taylor, allows for improvements in image processing and image quality. Claim 39 is not considered to stand and fall independently Appellant has repeated the argument provided for claim 29. A separate argument must be provided and argued for each claim.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Anner Holder/

Examiner, Art Unit 2621

June 4, 2009

Conferees:

/Andy S. Rao/

Acting Supervisory Patent Examiner, Art Unit 2621

/Thai Tran/

Supervisory Patent Examiner, Art Unit 2621